sensing when the first primary power output voltage reaches or exceeds a threshold reference level; and

delaying connection of the power supply controlled voltage power outputs for a selected delay time after the first primary power output voltage reaches the reference threshold level.

12. (Previously presented) The method of claim 11 further comprising, generating an output signal indicating that the first primary power voltage has reached at least 90% of its target value.

13. (Previously presented) The method of claims 11, wherein the step of comparing a signal representative of the first primary power voltage to a reference voltage further comprises:

dividing a signal representative of the first primary power voltage and comparing the voltage divided signal to a threshold reference voltage.

14. (Previously presented) The method of claim 13 wherein the delaying step comprises timing an interval starting when the voltage divided signal exceeds the threshold reference signal and delaying connection of the controlled voltage power outputs to the computer for a selected delay time.

15. (Original) The method of claims 11 further comprising ~~linerally~~ linearly controlling each of the power output voltages of the power monitor circuit.

16. (Previously presented) A power monitor circuit comprising:

a first input adapted to receive a first primary voltage from a power supply;

one or more secondary inputs to receive one or more secondary primary voltages from the power supply, wherein the one or more secondary primary voltages are related to the first primary voltage;

a comparator circuit adapted to compare the first primary voltage with a reference voltage; and

a time delay circuit adapted to delay an output of the one or more secondary primary voltages by a select period of time once the first primary voltage equals or exceeds the reference voltage.

17. (Currently amended) The power monitor circuit of claim 16, wherein the comparator circuit further comprises:

a resistor divider network adapted to divide the first primary voltage, the resistor divider network comprising:

a first resistor of a first select value, and

a second resistor of a second select value, the first and second resistor being adapted to divide the first primary voltage into a select first divided primary voltage; and

a comparator having a first input coupled to the ~~resister~~ resistor divider network to receive the select divided first primary voltage, the comparator having a second input coupled to receive the reference voltage, the comparator further having an output coupled to the time delay circuit.

18. (Previously presented) The power monitor circuit of claim16, wherein the reference voltage is approximately equal to 90% of the first primary voltage.

19. (Previously presented) The power monitor circuit of claim 16, wherein the time delay circuit outputs the first primary and one or more secondary primary voltages approximately 40ms after the primary voltage equals or exceeds the reference voltage.

20. (Previously presented) The power monitor circuit of claim 16, wherein the first primary voltage is approximately equal to 12 volts, one of the secondary primary voltages